Amplitude Equalizers – Types and Design

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Abstract -- **Various types of amplitude equalizers (AEs) and their designs are reviewed. First the design of voltage mode AEs derived from specific OA circuits is described. Design of one of these circuits allows the realization of AEs for specified whole range and the value of variable resistance at which the flat response is obtained. However, there is a limited flexibility of choosing the shaping function *H*(*s*). Then the block diagram approach, where one can choose *H*(*s*) is presented. Next, AEs with other devices, such as FTFN, CFA, Current conveyors, etc. are derived. Then voltage mode AEs, which have virtual ground, are converted in to current mode AEs. Two additional current mode AEs are also included.**

Keywords: Equalizers, Voltage mode, Current mode, Current conveyers.

I. INTRODUCTION

THE amplitude equalizers (AEs) are used in many systems to compensate for the deviations produced in the loss-gain response. Bode [1] suggested, for realizing AE, the transfer function

$$T(s) = \frac{1 + xH(s)}{x + H(s)} \tag{1}$$

where x is a function of a single variable resistor R_v and is dimensionless. For any AE, $T(s)$ should satisfy the following relations.

$$T(s) = \begin{cases} 1/H(s) & \text{for} \quad R_\upsilon = R_{\upsilon 1} = 0 \\ H(s) & \text{for} \quad R_\upsilon = R_{\upsilon 2} = \infty \\ 1 & \text{for} \quad R_\upsilon = R_f \end{cases} \tag{2}$$

From eqn. (1), the following properties are noted.

1. It has a symmetry around 0 dB line and has flat response for $R_v = R_f$.
2. As x varies from 0 to ∞, $T(s)$ varies from $1/H(s)$ to $H(s)$. The *whole range* (WR) is defined as a difference in the values of the variable resistance R_v when $T(s) = H(s)$ and $1/H(s)$. Thus, the WR is ∞.
3. The x and $H(s)$ are interchangeable.
4. When $H(s)$ is replaced by $1/H(s)$, $T(s)$ becomes $1/T(s)$. Hence, one has to consider the realization of either $T(s)$ or $1/T(s)$.
5. A flat response, $T(s) = 1$, is obtained when $x = 1$. The corresponding value of R_v is designated as RF.

II. DESIGN

Analysis-based Design: Choose a suitable circuit and find its transfer function $T(s)$. Now there are following two approaches.

Approach 1: Arrange it in the form as

$$T(s) = K\frac{1 + x_a H_a(s)}{x_b + H_b(s)} \tag{3}$$

Compare eqn. (3) with eqn. (1) and get the following relations.

$K = 1$, $x = x_a$, for $H = H_a$, and $x = x_b$, for $H = H_b$,

Since there are only 3 equations, unknowns more than 3 can be suitably assumed.

Approach 2: Find three conditions from eqn. (3) as per the relations given in eqn. (2) and solve for the values of various components. Unknowns more than 3 can be suitably assumed.

We will use one or the other method in the following types of AEs.

Type I: Consider the circuit shown in Fig. 1. Analysis gives

$$T_1 = \frac{V_o}{V_i} = \frac{Z(R_a + R_b) + R_a R_b + ZR}{Z(R_a + R_b) + R_a R_b + ZR + R_a R}$$
$$= \frac{Z(R_a + R_b) + R_a R_b + ZR}{(Z + R_a)R + Z(R_a + R_b) + R_a R_b}$$

$$\left[\frac{Z(R_a + R_b) + R_a R_b}{(Z + R_a)Ra}\right] \frac{\left[1 + \left(\frac{R}{R_a}\right)\left(\frac{Z}{Z\left(1 + \frac{R_b}{R_a}\right) + R_b}\right)\right]}{\left[\frac{R}{R_a} + \frac{Z\left(1 + \frac{R_b}{R_a}\right) + R_b}{(Z + R_a)}\right]} \tag{4}$$

Let

$$\frac{Z(R_a+R_b)+R_aR_a}{(Z+R_a)R_a}=1, \qquad (5)$$

$$\Rightarrow ZR_b = R_a(R_a - R_b)$$

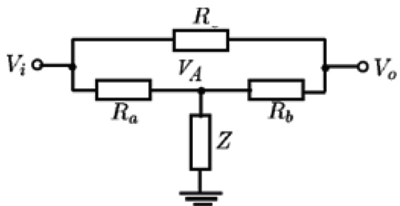


Figure 1. Passive circuit.

Equation (5) *demands* $R_a = R_b = 0$*, which is not admissible.* To overcome this difficulty, we take

$R = R_v - R_o$.

Now eqn. (4) becomes

$$T_2(s)=\left[\frac{Z(R_a+R_b-R_o)+R_aR_b}{(Z+R_a)R_a}\right]\frac{\left[1+\left(\frac{R_v}{R_a}\right)\left(\frac{Z}{Z\left\{1+\frac{R_b-R_o}{R_o}\right\}+R_b}\right)\right]}{\left[\frac{R_v}{R_a}+\frac{Z\left\{1+\frac{R_b-R_o}{R_o}\right\}+R_b-R_o}{(Z+R_a)}\right]} \qquad (6)$$

Let

$$\frac{Z(R_a+R_b-R_o)+R_aR_b}{(Z+R_a)R_a}=1 \qquad (7)$$

$$x_2=\frac{R_v}{R_a} \qquad (8)$$

$$H_2(s)=\frac{Z}{Z\left(1+\frac{R_b-R_o}{R_a}\right)+R_b}=\frac{Z\left(1+\frac{R_b-R_o}{R_a}\right)+(R_b-R_o)}{Z+R_a} \qquad (9)$$

Now eqn. (7) demands

$$Z(R_b-R_o)=R_a(R_a-R_b).$$

This can be satisfied only if

$$R_a=R_b=R_o$$

Then eqn. (6) reduces to

$$x_2=\frac{R_v}{R_o} \qquad (10)$$

and eqn. (9) to

$$H_2=\frac{Z}{Z+R_o} \qquad (11)$$

Finally,

$$T_2(s)=\frac{1+x_2H_2}{x_2+H_2}$$

Thus, the circuit reduces to that shown in Figure 2 which is the same as proposed by Saraga and Zyoute [2]. The fixed negative resistance $-R_0$ can be simulated using a negative resistance converter. Since the negative resistance is a floating one, it will require too many components to simulate it. The circuit requires an additional buffer at the output to avoid loading. The WR of this AE is ∞.

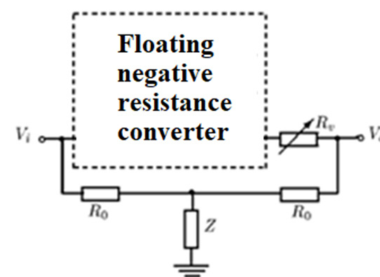


Figure 2. AE 1 (Saraga and Zyoute [2]).

Type II: Consider the circuit shown in Fig. 3(*a*). Analysis gives

$$T_3(s)=\frac{R-\frac{R_b}{R_a}Z}{R+Z} \qquad (12)$$

Let

$$R_a=R_b=R_o \qquad (13)$$

Then

$$T_3(s)=\frac{R-Z}{R+Z}=\frac{2R_o(R-Z)+(R_o{}^2+RZ)-(R_o{}^2+RZ)}{2R_o(R-Z)+(R_o{}^2+RZ)-(R_o{}^2+RZ)}$$

$$=\frac{1+\left(\frac{R+R_o}{R-R_o}\right)\left(\frac{R_o-Z}{R_o+Z}\right)}{\left(\frac{R+R_o}{R-R_o}\right)+\left(\frac{R_o-Z}{R_o+Z}\right)}=\frac{1+x_3H_3}{x_3+H_3} \qquad (14)$$

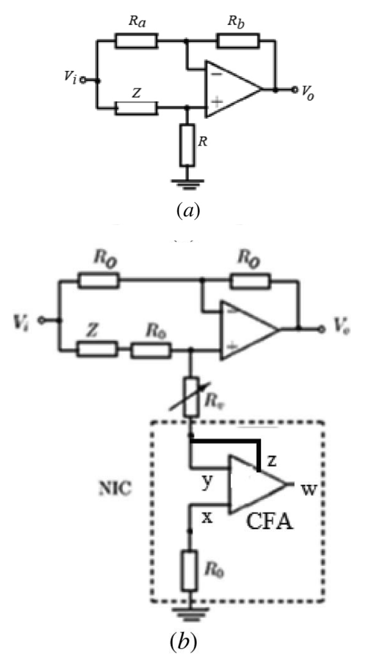


Figure 3. (*a*) Active circuit and (*b*) AE 2 (Brglez[3]).

where

$$x_3 = \frac{R + R_o}{R - R_o} \tag{15}$$

and

$$H_3 = \frac{R_o - Z}{R_o + Z} \tag{16}$$

Thus, we note that any first order all-pass transfer function (when Z = 1/*sC*) can be converted into an AE function by introducing R_o.

From eqn. (16), note that for x_3 to vary from 0 to ∞ so that $T_3(s)$ varies from $1/H_3(s)$ to $H_3(s)$, R should vary from $-R_0$ to $+R_0$. Thus WR is $2R_0$. Since, *a practical variable resistor cannot have negative value*, we take

$$R = R_v - R_o \tag{17a}$$

In view of eqn. (17*a*) and (14) becomes

$$T_3(s) = \frac{1 + \left(\frac{R_v}{R_v - 2R_0}\right) H_3(s)}{\frac{R_v}{R_v - 2R_0} + H_3(s)} \tag{17b}$$

The $T_3(s)$ now varies from $1/H_3(s)$ to $H_3(s)$ when R_v varies from 0 to $2R_0$. Thus, the WR remains the same $2R_0$. A flat response is obtained when $R_v = R_0$. Thus the circuit shown in Fig. 3(*a*) leads to the circuit shown in Fig. 3(*b*) which is the same as given by Brglez [3]. It may be noted that the Brglez Circuit uses *Z* as a series combination of the fixed resistance R_o and impedance *Z*. This splitting of *Z* may not be required.

NIC is simulated using a CFA as shown in Figu. 3(*b*) [4]. To eliminate the NIC in the circuit of Fig. 3(*b*), Brglez [5] used a switch as shown in Fig. 4. The circuit provides the positive R_v range when the switch is connected to A terminal and the negative R_v range when connected to B terminal. One can see that the toggling of the switch provides basically two inverse active networks [6].

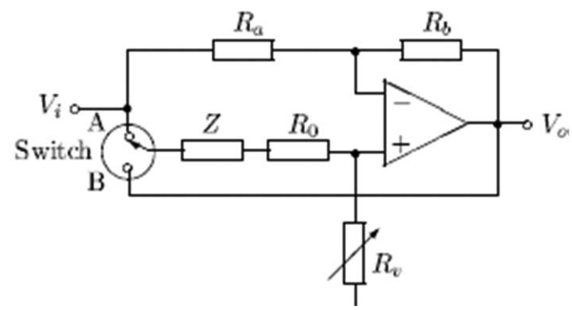


Figure 4. AE 2 (Brglez AE with a switch).

Type III: Consider the circuit [7] shown in Fig. 5.

The analysis of the circuit gives

$$T_4(s) = \left[\frac{Z + R_b}{Z + R_c + R_e}\right] \frac{\left[1 + \left(\frac{R_v}{R_e}\right)\left(\frac{Z + R_e - \frac{R_b R_c}{R_a}}{Z + R_b}\right)\right]}{\left[\frac{R_v}{R_e} + \frac{Z}{Z + R_c + R_e}\right]}. \tag{18a}$$

Design 1: Let

$$\frac{Z + R_b}{Z + R_c R_e} = 1 \tag{18b}$$

$$\rightarrow R_b = R_c + R_e, \tag{19}$$

and

$$x_4 = \frac{R_v}{R_e}, \tag{20}$$

$$H_4(s) = \frac{Z}{Z + R_b} = \left(\frac{Z + R_e - \frac{R_b R_c}{R_a}}{Z + R_b}\right) \tag{21}$$

$$\rightarrow R_b = \frac{R_a R_e}{R_c}. \tag{22}$$

Equating the two values of R_b from eqn. (19) and eqn. (22), we get

$$R_c^{\,2} + R_e R_c - R_a R_e = 0. \tag{23}$$

Solving for R_c, we get

$$R_c = \frac{-R_e \pm \sqrt{R_e^2 + 4R_aR_e}}{2} \tag{24}$$

$$T_4(s) = \frac{1 + \left(\frac{R_v}{R_e}\right)\left(\frac{Z}{Z+R_b}\right)}{\left(\frac{R_v}{R_e}\right) + \left(\frac{Z}{Z+R_b}\right)}$$

Equations (23) and (24) are the design relations for AE of Figure 5(a), after choosing suitable

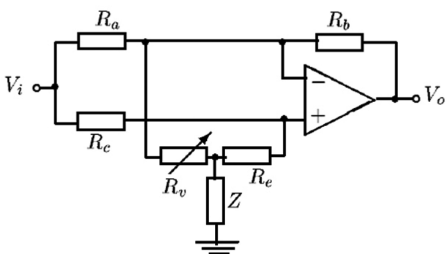


Figure 5. AE 3.

Value for R_a. Thus, there are *many possible AEs*. Two of them are given below.

(*a*) AE 3(*a*) Let $R_a = 2R_e$. Then $R_c = R_e$, $R_b = 2R_e$. This circuit is the same as given by Zyoute [7] when $R_e = R_o$.

(*b*) AE 3(*b*): Let $R_a = (15/4)R_e$. Then $R_c = (3/2)R_e$, $R_b = (5/2)R_e$.

Design 2: Equation (17) can be rearranged as

$$T_5(s) = K\frac{1 + x_a H_5(s)}{x_b + H_5(s)} \tag{25}$$

where

$$K = \frac{1 + \dfrac{R_vR_aR_bR_e - R_b^2R_cR_v - R_vR_aR_eZ}{R_aR_bR_e(Z+R_b)}}{1 - \dfrac{R_v}{R_b}}, \tag{26}$$

$$x_a = \frac{\dfrac{R_v}{R_b}\left(1 + \dfrac{R_b}{R_e}\right)}{\dfrac{\left(1 - \dfrac{R_v}{R_b}\right)\left(Z + \dfrac{R_b - \dfrac{R_bR_cR_v}{R_aR_e} + R_v}{1 - \dfrac{R_v}{R_b}}\right)}{(Z+R_b)}} \tag{27}$$

$$x_b = \frac{\left[\dfrac{R_v}{R_b}\right]\left[1 + \left(\dfrac{R_b}{R_e}\right)\left(\dfrac{Z+R_c}{Z+R_b}\right)\right]}{1 - \dfrac{R_v}{R_b}} \tag{28}$$

and

$$H_5(s) = \frac{Z}{Z+R_b} \tag{29}$$

Let

$$x_5 = x_a = x_b, \tag{30}$$

i.e.,

$$x_5 = \frac{\dfrac{R_v}{R_b}\left(1 + \dfrac{R_b}{R_e}\right)}{\dfrac{\left(1 - \dfrac{R_v}{R_b}\right)\left(Z + \dfrac{R_b - \dfrac{R_bR_cR_v}{R_aR_e} + R_v}{1 - \dfrac{R_v}{R_b}}\right)}{(Z+R_b)}}$$

$$= \frac{\dfrac{R_v}{R_b}\left[1 + \left(\dfrac{R_b}{R_e}\right)\left(\dfrac{Z+R_c}{Z+R_b}\right)\right]}{1 - \dfrac{R_v}{R_b}} \tag{31}$$

For x_5 to be independent of Z, eqn. (30) requires

$$R_b = \frac{2R_aR_e}{R_c} \tag{32}$$

and

$$R_b = R_c = R_o \tag{33}$$

Equating the two values of R_b from eqns. (32) and (33), we get

$$R_c = \sqrt{2R_aR_e}. \tag{34}$$

Under these conditions eqn. (25) gives

$K = 1$.

Thus from eqn. (30)

$$x_5 = \frac{\dfrac{R_v}{R_b}\left[1 + \left(\dfrac{R_b}{R_e}\right)\right]}{1 - \dfrac{R_v}{R_b}} = \frac{R_b + R_e}{\dfrac{R_bR_e}{R_v} - R_e}. \tag{35}$$

Now eqn. (25) becomes

$$T_5(s) = \frac{1 + x_5 H_5(s)}{x_5 + H_5(s)} \tag{36}$$

where H_5 and x_5 are given by eqn. (29) and (35), respectively. From eqn. (35), note that $T_5(s)$ varies from $1/H_5(s)$ to $H_5(s)$ when R_v varies from 0 to R_o. Thus, the WR becomes R_o.

The design steps are the following.

(*i*) Choose R_a and R_e.
(*ii*) Find R_c from eqn. (34)
(*iii*) Find R_b from eqn. (32).

(*a*) AE 3(*c*): Let $R_a = R_o/2$, $R_e = R_o$, then $R_c = R_b = R_o$. The circuit becomes the same as depicted by Talkhan *et al*. [8].

(*b*) AE 3(*d*): Let $R_a = 2R_e$, $R_e = R_o$, then we get $R_b = R_c = 2R_e$.

Design 3: Equation (17) can be rearranged as

$$T_6(s)=\frac{Z+\frac{R_aR_bR_e+R_v(R_aR_e-R_bR_c)}{R_a(R_v+R_e)}}{Z+\frac{R_v(R_e+R_c)}{(R_v+R_e)}} \tag{37}$$

From eqn. (37),

$$T_6(s)_{R_v=0}=\frac{Z+R_b}{Z}=H(s) \tag{38}$$

$$T_6(s)_{R_v=R_r}=\frac{Z+\frac{R_aR_bR_e+R_r(R_aR_e-R_bR_c)}{R_a(R_r+R_e)}}{Z+\frac{R_r(R_e+R_c)}{(R_r+R_e)}}=\frac{1}{H(s)}=\frac{Z}{Z+R_b} \tag{39}$$

This is satisfied when

$$\frac{R_aR_bR_e+R_r(R_aR_e-R_bR_c)}{R_a(R_r+R_e)}=0 \tag{40}$$

$$\Rightarrow\ R_b=\frac{R_rR_eR_a}{R_rR_c-R_aR_e} \tag{41}$$

and

$$R_b=\frac{R_r(R_e+R_c)}{(R_r+R_e)} \tag{42}$$

Equating two values of R_b from eqns. (45) and (46), we get

$$R_a=\frac{R_cR_r(R_e+R_c)}{R_e(R_r+2R_e+R_c)} \tag{43}$$

Condition for flat response, from eqn. (36), is

$$T_6(s)_{R_v=R_f}=\frac{Z+\frac{R_aR_bR_e+R_f(R_aR_e-R_bR_c)}{R_a(R_f+R_e)}}{Z+\frac{f(R_e+R_c)}{(R_f+R_e)}}=1 \tag{44}$$

$$\Rightarrow R_e=\frac{R_fR_r}{R_r-2R_f} \tag{45}$$

For R_e to be non-negative real,

$$R_r\geq 2R_f \tag{46}$$

However, when $R_r = 2R_f$, $R_e \to \infty$.

Thus

$$T_6(s)\Big|_{R_r=2R_f}=\frac{Z+R_b+R_f}{Z+R_f}>1 \tag{47}$$

and eqn. (43) is not satisfied. Therefore

$$R_r > 2R_f\,. \tag{48}$$

Equations (42), (43) and (45) are the design equations with restrictions given by eqn. (48).

Let

$$R_b = R_O. \tag{49}$$

Then from eqn. (42), we get

$$R_c=R_o+\left(\frac{R_o}{R_r}-1\right)R_e. \tag{50}$$

Design procedure, when R_r and R_f are specified, is as follows [9].

Find R_e from eqn. (45), R_b from eqn. (49), R_c from eqn. (50) and R_a from eqn. (43).

Following the above procedure, AE-3(*e*)- AE 3(*i*) are designed for five different sets of values of R_r and R_f and results are given in Table 1. Value of x is obtained from x_6 given in eqn. (35).

AE 3(*e*) is the same as that of Zyoute [7]. However, he has chosen the value of R_e, and therefore, R_f gets fixed as per eqn. (45). AEs 3(*f*) and 3(*g*) were considered in [8] where different values of R_e gives different R_f as per eqn. (45), but R_r remains the same. In [7] and [8], R_e or R_a was chosen instead of finding it from eqn. (45) or eqn. (43).

It may be noted that the design is applicable for both the fan and bump equalizers and also for the inverse networks [6].

More complex AEs

Type IV: AE-4 proposed by Nowrouzian and Fuller [10] is, after correction, shown in Fig. 6. Analysis of the circuit yields

$$H_7(s)=\frac{R_0+Z}{R_0-Z} \tag{51}$$

It requires, after including one missing inverter in their circuit, 5 OAs and 14 resistors. In the circuit of Fig. 6(*b*), one cannot isolate the block $H_7(s)$.

TABLE 1 -- DESIGN OF EQUALIZERS FOR FIVE SETS OF R_r AND R_f, WITH $R_b = R_o$

	R_r	R_f	R_e	R_c	R_a	x
AE 3(e)	∞	$\frac{1}{2}R_0$	$\frac{1}{2}R_0$	$\frac{1}{2}R_0$	R_0	$\frac{2R_v}{R_0}$
AE 3(f)	R_0	$\frac{1}{3}R_0$	R_0	R_0	$\frac{1}{2}R_0$	$\frac{2R_v}{R_0 - R_v}$
AE 3(g)	R_0	$\frac{1}{4}R_0$	$\frac{1}{2}R_0$	R_0	R_0	$\frac{3R_v}{R_0 - R_v}$
AE 3(h)	$\frac{1}{2}R_0$	$\frac{1}{8}R_0$	$\frac{1}{4}R_0$	$\frac{5}{4}R_0$	$\frac{5}{3}R_0$	$\frac{6R_v}{R_0 - 2R_v}$
AE 3(i)	$\frac{1}{4}R_0$	$\frac{1}{10}R_0$	$\frac{1}{2}R_0$	$\frac{5}{2}R_0$	R_0	$\frac{6R_v}{R_0 - 4R_v}$

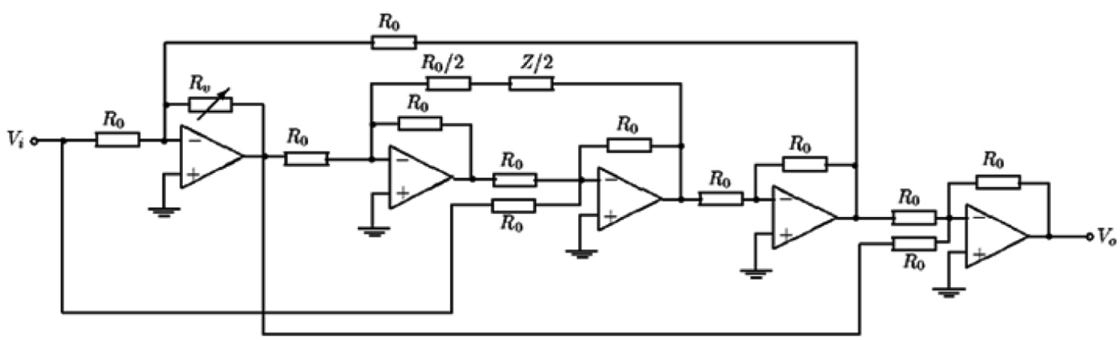


Figure 6. AE 4.

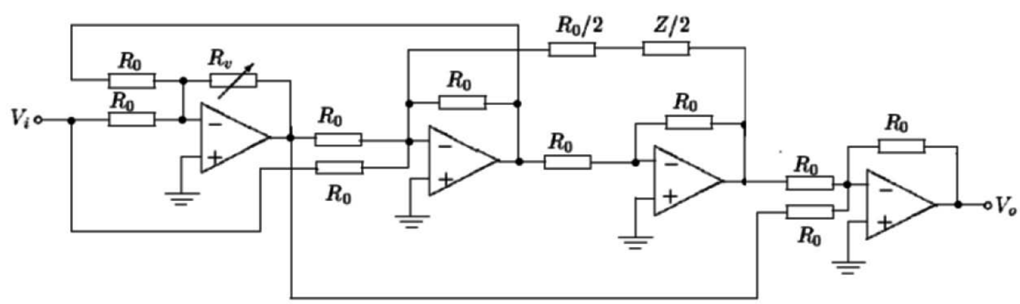
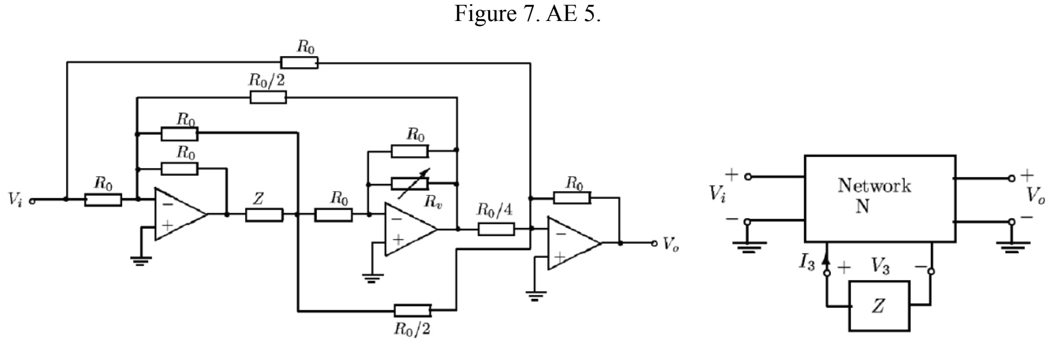


Figure 7. AE 5.



(a) (b)

Figure 8. AE 6.

TABLE 2 -- A COMPARISON OF VARIOUS AEs

AEs	No		WR	$H(s)$
	OAs	Resistors		
Saraga and Zyoute AE [2]	01	06	∞	
Brglex AE [3]	02	08	$2R_0$	$R_0/(Z+R_0)$
Zyoute AE [7]	01	05	∞	$Z/(Z+2R_0)$
Talkhan AE [8]	01	05	R_0	$Z/(Z+R_0)$
Nowrouzian and Fuller AE [10]	05	14	∞	$\frac{R_o+Z}{R_o-Z}$
Nowrouzian *et al.* AE [11]	03	11	∞	$\frac{2Z}{2Z+R_o}$
Rathore and Khot AE [13]	04	12	∞	$\frac{R_o+Z}{R_o-Z}$

Type V: AE 5, with the similar performance as AE 4, but with reduced number of components, is shown in Fig. 7.

Type VI: AE 6, proposed by Nowrouzian *et al.* [11], is shown in Fig. 8. The analysis of the circuit leads to

$$T_7(s) = -\frac{\frac{R_v}{R_0}+\frac{2Z}{2Z+R_0}}{1+\left(\frac{R_v}{R_0}\right)\frac{2Z}{2Z+R_0}} = -\frac{x_7+H_7(s)}{1+x_7 H_7(s)} \quad (52)$$

where

$$x_7 = \frac{R_v}{R_0} \quad (53)$$

and

$$H_7(s) = \frac{2Z}{2Z+R_0} \quad (54)$$

Block diagram approach

In all the above types of AEs, there is very limited flexibility of choosing $H(s)$ by choosing Z(s). Now we will introduce AEs which can have any desired $H(s)$ [12]. The block diagram of the function

$$T_7(s) = \frac{\frac{R_v}{R_o}+H_7(s)}{1+\frac{R_v}{R_o}H_7(s)} \quad (55)$$

is given in Fig. 9. Note that we have chosen all summers with inverting type so that they can be realized by inverting type OA configuration. Since there are four summers, we will require minimum 4 OAs.

Type VII: Based on the block diagram, one possible realization of is shown in Fig. 10(a). In this circuit

$$x_7 = \frac{R_v}{R_o} \quad (56)$$

One may choose

$$H_7(s) = \frac{R_o+Z}{R_o-Z} \quad (57)$$

A circuit for realizing $H_7(s)$ is shown in Fig.10(b) with non-inverting terminals of all the OAs grounded. If this $H_7(s)$ block of Fig. 10(c) is inserted into the main circuit in Fig. 10(a), one inverter and one summer can be eliminated. Thus the circuit can be reduced to that of [10].

Type VIII: One may choose

$$H_8(s) = \frac{1}{H_7} = \frac{R_o-Z}{R_o+Z}. \quad (58)$$

Then

$$T_8(s) = \frac{1}{T_7(s)} = \frac{1+\frac{R_v}{R_o}H_8(s)}{\frac{R_v}{R_o}+H_8(s)} \quad (59)$$

The realization is obtained by inverse transform [6] on Fig. 10(b) and shown in Fig. 10(c).

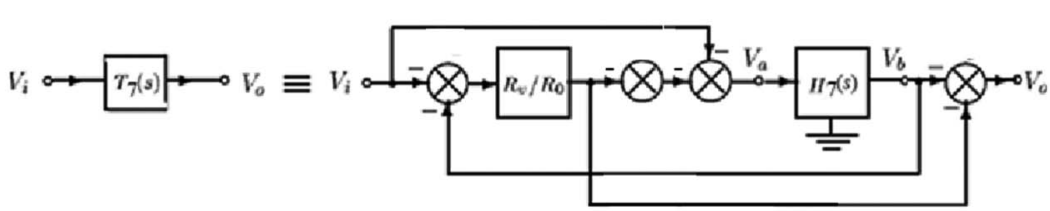


Figure 9. Block diagram of T_7 (s).

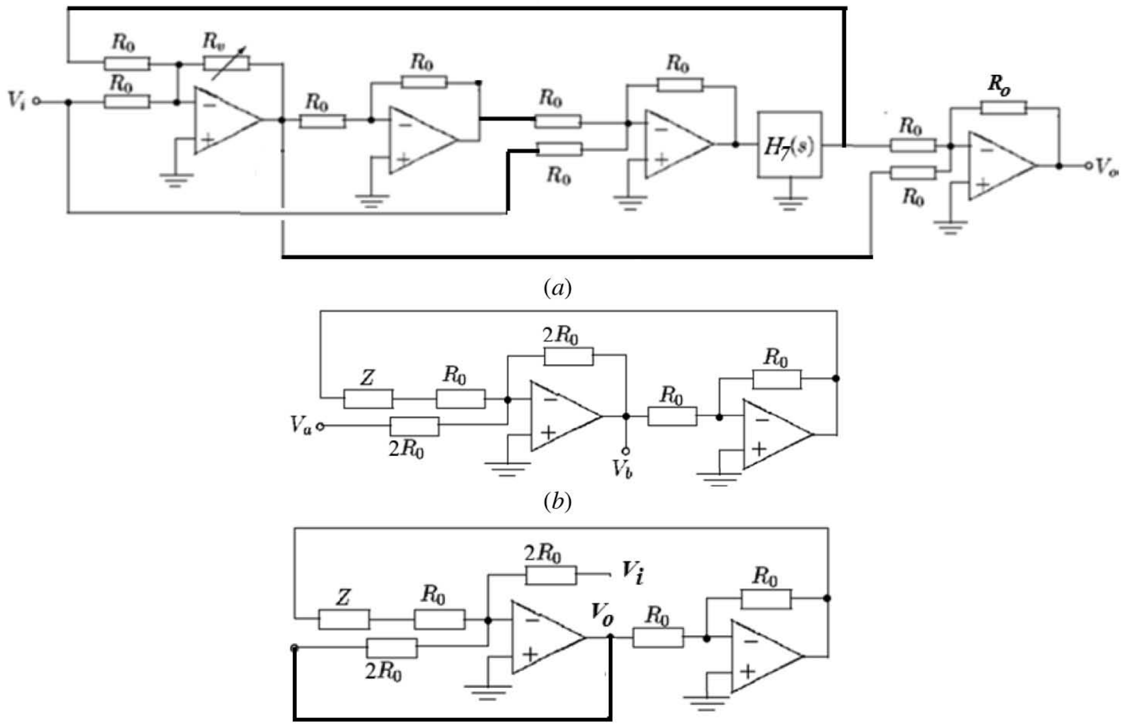


Figure 10. Active RC realizations of (*a*) $T_7(s)$, (*b*) $H_7(s)$ and (*c*) $1/H_7$(s).

AES with other active devices

Type IX

Circuit VII: The OA based AE shown in Fig. 5 (reproduced in Fig. 11(*a*) can be transformed into circuits employing other active devices. Two such circuits employing active devices having terminal characteristics $V_x = V_y$, $I_z = I_x$ and $I_y = 0$ are derived and shown in Fig. 11(*b*) and 11(*c*).

From figures 11(*a*), (*b*) and (*c*), we can write, respectively,

$$I = I_1 + I_2 = \left(\frac{V_x}{R_b} - \frac{V_o}{R_b}\right) + I_2 \tag{60}$$

$$\begin{aligned} I &= I_1 + I_2 = (I_x + I_z) + I_2 \\ &= 2I_z + I_2 = 2\left(\frac{V_x}{R} - \frac{V_o}{R}\right) + I_2 \end{aligned} \tag{61}$$

$$\begin{aligned} I &= I_1 + I_x + I_2 = I_1 + I_z + I_2 \\ &= \left(\frac{V_x}{R_1} - \frac{V_o}{R_2}\right) + I_2 \end{aligned} \tag{62}$$

For the circuits shown in Figs. 11(*a*) and (*b*) to be equivalent to that shown in Fig. 11(*a)*, eqns. (60) and (61) require

$$R=2R_b \tag{63}$$

and from eqns. (60) and (62),

$$R_1=R_2=R_b \tag{64}$$

Although the circuit of Fig. 13(*c)* requires one more resistance than that shown in Fig. 13(*b)*, the total resistance is the same.

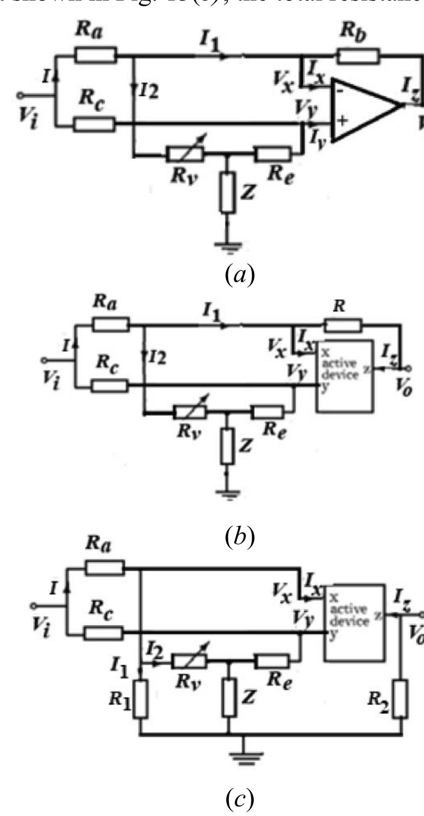


Figure 11. (*a*) OA-based AE, (*b*) and (*c*) Two AEs derived from (*a*).

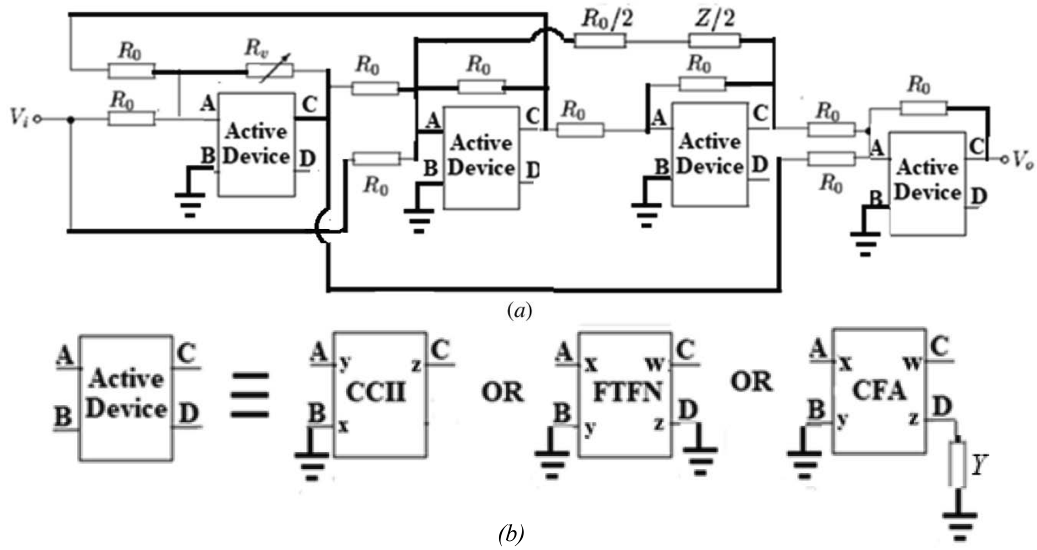


Figure 12 (*a*) VM AE obtained from the AE of Fig. 12 and (*b*) Some active devices.

Type X**:** Another type of AEs derived from OA-based circuit of Fig. 7 is shown in Fig. 12(*a)* [14]. Some of the active devices are shown in Fig. 12(*b*). In case of CFA an admittance *Y* is added at terminal D, which is a part of the feedback admittance connected across AC. The terminal characteristics of CCII, FTFN and CFA, respectively, are

$$\begin{bmatrix} V_x \\ I_z \\ I_y \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}, \quad \begin{bmatrix} V_x \\ I_z \\ I_y \\ V_w \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ I_w \\ V_z \end{bmatrix}, \quad \begin{bmatrix} V_x \\ I_z \\ I_y \\ I_x \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_w \\ V_w \\ V_z \end{bmatrix} \tag{65}$$

Current mode AEs using VM-CM transformation

Type XI: Using VM-to-CM transformation method [13], one can convert the OA based VM AE of Fig. 7 into CM AE as show in Fig. 13(*a)* with different active devices as shown in Fig. 13(*b)* [14]. The terminal characteristic of OA is $V_x = V_y$, $I_x = I_y = 0$. The characteristics of other devices are given in eqn. (65).

Type XII

Now, consider the circuit using CDBA ($V_x = 0$, $V_y = 0$, $I_z = I_y - I_x$, $V_w = V_z$) as shown in Fig. 14(*a*). The analysis of the circuit leads to

$$T(s) = \frac{I_o}{I_i} = \frac{\dfrac{R_\upsilon}{Z} - 1}{\dfrac{R_\upsilon}{Z} + 1} \tag{66}$$

This *T*(*s*) is in similar form as that given in eqn. (17) when $R_a = R_b$. Following the similar technique used for realizing Brglez's AE, we get

$$T(s) = \frac{1 + \left(\dfrac{R_p}{R_p - 2R_0}\right)\left(\dfrac{R_0 - Z}{R_0 + Z}\right)}{\dfrac{R_p}{R_p - 2R_0} + \dfrac{R_0 - Z}{R_0 + Z}} \tag{67}$$

where $R_v = R_p - R_o$.

Comparing eqn. (67) with eqn. (1), we get

$$x = \frac{R_p}{R_p - 2R_0} \tag{68}$$

and

$$H(s) = \frac{R_0 - Z}{R_0 + Z} \tag{69}$$

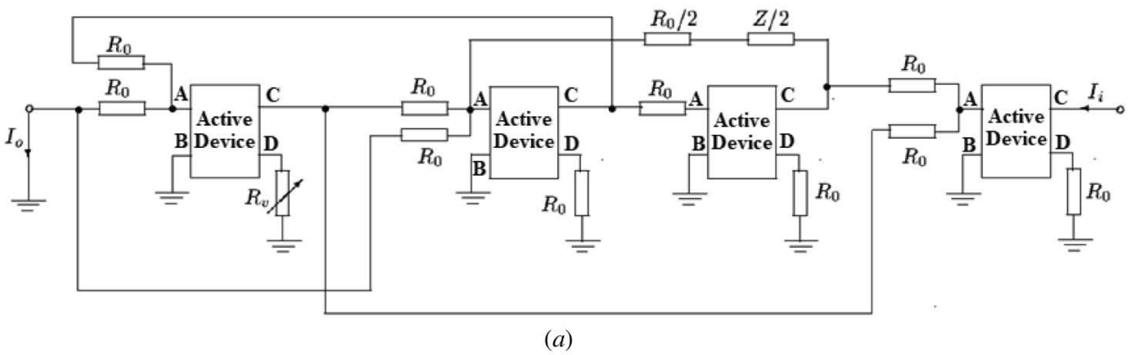
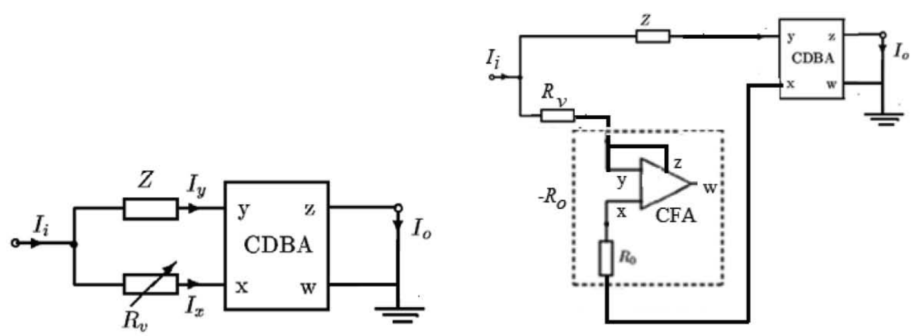


Figure 13 (*a*). CM AEs derived from VM AE of Figure 7, (b) Some active devices.



(*a*) (*b*)

Figure 14. CM AEs employing (*a*) one CDBA, (*b*) one CDBA and one NIC.

The complete CM AE is shown in Fig. 14(*b)*. The negative resistance R_o is simulated as shown in the figure. The WR of the AE is $2R_o$.

III. CONCLUSION

In this review paper, various types of amplitude equalizers (AEs) and their designs have been presented. First, the design of voltage mode AEs derived from specific OA circuits is described. Design of one of these circuits allows the realization of AEs for specified whole range (WR) and the value of variable resistance (RF) at which the flat response is obtained. However, there is a limited flexibility of choosing the shaping function $H(s)$. The block diagram approach, where one can choose $H(s)$, has been given. Next, AEs with other devices, such as FTFN, CFA, Current conveyors, etc. are presented. Voltage mode AEs, which have virtual ground, have been converted in to current mode AEs. Two additional current mode AEs are also presented.

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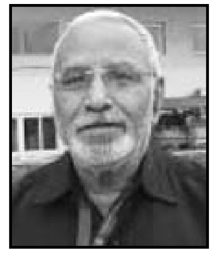

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